**Abstract**

A tri-level decoder circuit includes a first decoder circuit and a second decoder circuit. The first decoder circuit is configured to compare an input voltage to a first threshold, and the second decoder circuit is configured to compare the input voltage to a second threshold. The first decoder circuit is configured to provide substantially no current to a current mirror if the input voltage is less than the first threshold, and to provide a current to the current mirror otherwise. The current mirror is configured to reflect the current to provide a reflected current. A current source is configured to pull down a first output node to a first logic level if the reflected current is substantially zero. The current mirror is configured to drive the first output node to a second logic level otherwise. The second decoder circuit may operate similarly.